Junior Purdue Student

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Education

Purdue University Indiana, US| Class of 2026

Bachelor of Science, Computer Engineering (BSCMPE) GPA: 3.81

-Relevant Courses: ASIC Design Laboratory, Digital System Design, Data Structures, Python for Data Science

-Upcoming Courses (S24): Microprocessor System & Interfacing, Computer Design and Prototyping, Operating Systems

Experience

Western Digital Corporation California, US

Product Design Engineering Intern June 2024 – August 2024

- Developed and implemented AutoEncoder ML model for anomaly detection reducing die DPPM by # (or time)
- Optimized Analog DFT flows, identifying critical threshold voltage bounds, resulting in yield increase of #
- Proposed ANOVA outlier clipping, reducing yield loss by #% by logically combining multiple test parameters
- Designed comprehensive training material on charge trap MOSFET, NAND array, and BiCS6 3D technology

USB Full-Speed Bulk-Transfer AHB-Lite SOC Indiana, US

Team Lead & AHB Designer January 2024 – May 2024

- Developed and integrated top-level & Bus RTL to facilitate host & endpoint transfers via 64 Byte FIFO Data Buffer
- Managed pipelined host requests and TX/RX buffer usage through 8-bit packets and 10 flags using control FSM
- Developed comprehensive UVM with # testcases, identifying # bugs, resulting in #hours reduced in development
- Co-developed Python verification script, converting endpoint data parity bits into 8-byte AHB HREAD data-line

NanoXLab Indiana, US

Undergraduate *Researcher (System to Device Modeling)* May 2023 – Current

- Analyzed 1/f & RTN induced effects on data retention at high temperature using Stanford SystemX's RRAM device
- Initiated development of a predictive framework leveraging device physics and DNNs for industry applications
- Conducted research on Meta's Carbon Explorer framework and advancements in Neuromorphic Computing

Summer Training, Awareness, and Readiness for Semiconductors (STARS) Indiana, US

Design Track - Memory Calculator Team May 2023 – July 2023

- Developed and prototyped memory calculator using SystemVerilog, verified across 3 iterations of FPGA iterations
- Created testbench scripts for ALU, Shift Register, Read & Write FSM modules, enhancing reliability of calculator
- Successfully managed project timeline, saving 20 total hours, improving team efficiency with workload allocation
- Synthesized the design into GDS file, optimizing layout to utilize 4.5% of the specified area constraint

Computer Vision Object and Feature Detection (Python) Indiana, US

P*roject Manager* October 2022

- Led a 7-day project sprint using Excel to define and track customized, measurable goals achieving project delivery
- Organized formal documentation of project motivation, overview, methods, algorithm design and references
- Coordinated development & debugging of 3 detection methods without OpenCV – SSDiff, CrossCoef, NormCCorr

Engineering Projects in Community Service (EPICS) Children Educational Displays Indiana, US

Project Manager & Design Team CAD Specialist (Simulated Space Travel) August 2023 – May 2023

- Supervised assembly and delivery of three displays, ensuring quality & specs. of Indianapolis Children's Museum
- Conducted weekly meetings resolving emerging issues and maintaining project momentum within a team of 16
- Developed all 3D printed prototypes and simulated track, magnet, & rocket dimensions w/ Autodesk Fusion 360

Singapore Armed Forces Singapore

42SAR Kaffir Company Armor Infantry Section Leader July 2020 – July 2022

- Led section assault missions, effectively integrating newly issued AFV: Hunter, improving operational readiness
- Engaged in physical training (4 hours/day) and theoretical & practical training hours (2 hours/day)

Additional Information

Technical skills: SystemVerilog | Python | TensorFlow | Keras | C | SQL | AWS Redshift | Data Structures

Interests: Semiconductors | AI/ML | Sustainable Technology | Golf | Latin & Ballroom Dance | Travelling